a host JTAG TAP controller coupled to each of the first JTAG TAP controllers.

22. (New) The system of Claim 21, wherein the FPGA-based SoC includes the host JTAG TAP controller.

23. (New) The system of Claim 21, further comprising:

a selector circuit coupled between the first JTAG TAP controllers and the host JTAG TAP controller.

24. (New) The system of Claim 23, wherein the FPGA-based SoC includes the host JTAG TAP controller and the selector circuit.

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25. (New) The system of Claim 21, wherein the host JTAG TAP controller comprises:

a selectable bit register having an input terminal coupled to the selector circuit and further having an output terminal providing a selected bit; and

an instruction register having an input terminal coupled to the output terminal of the selectable bit register, the instruction register having an output terminal providing an instruction having an apparently extended length.

26. (New) The system of Claim 25, further comprising:

a selector circuit coupled between the first JTAG TAP controllers and the host JTAG TAP controller.

27. (New) The system of Claim 25, wherein the FPGA-based SoC includes the host JTAG TAP controller.